jam

PTO/SB/08A (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application / Conf. No.	Unknown /
Filing Date	February 20, 2004
First Named Inventor	Kevin T. Look
Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	X-1462-2P US

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No.[1]	Document Number Number - Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 10/606,619		New et al.	Filed 6/26/2003
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No.[1]	Foreign Patent Document Country Code [3] -Number [4] -Kind Code [5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] See Kinds of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

PTO/SB/08A (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 2 of 2

Complete if Known	
Application / Conf. No.	Unknown /
Filing Date	February 20, 2004
First Named Inventor	Kevin T. Look
Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	X-1462-2P US

OTHER -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		HE, LEI; "Power Efficient FPGA: Circuit, Fabrics and CAD Algorithms," Presentation on February 13, 2004, 50 pages, at Xilinx, Inc. 2100 Logic Drive, San Jose, CA 95124, available from EE Department, UCLA, at http://eda.ee.ucla.edu/.	
		FPGA 2004 ADVANCE PROGRAM; "ACM/SIGDA Eleventh international Symposium on Field Programmable Gate Arrays, February 22-24, 2004, 6 pages, at Monterey Beach Hotel, Monterey, California, available at http://fpga2004.ece.ubc.ca/	
		INUKAI, T. et al., "Boosted Gate MOS (BGMOS): Device/Circuit Cooperation Scheme to Achieve Leakage-Free Giga-Scale Integration," 2000, pages 409-412, available from IEEE Journal of Solid-State Circuits, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997.	
		HAMZAOGLU, F. et al., "Circuit-Level Techniques to Control Gate Leakage for sub-100nm CMOS," ISLPED, August 12-14, 2002, Pages 60-63, available from IEEE Journal of Solid-State Circuits, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997.	
		KURODA, T., et al., "A 0.9V, 150-MHz, 1--mW, 4 mm^2 2-D Discrete Cosine Transform Core Processor with Variable Threshold-Voltage (VT) Scheme, 1996, pages 1770-1779, Vol. 31, No. 11, available from IEEE Journal of Solid-State Circuits, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997.	
		MUTOH, S. et al., "1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS," August 1995, pages 847-854, Vol. 30, No. 8, available from IEEE Journal of Solid-State Circuits, 3 Park Avenue, 17th Floor, New York, NY 10016-5997.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number. [2] Applicant is to place a check mark here if English language Translation is attached.